

(FILE 'USPAT' ENTERED AT 16:13:36 ON 06 AUG 95)

L1 5 S 4314332/UREF
E (KILLIAN, EARL A)/IN
L2 3 S E3
E (GOTOU, SHIZUO)/IN
L3 7 S E3
L4 3 S 4679140/UREF
L5 20 S ((VARIAB? OR ADJUST?) (4A) WIDTH# (4A) BIT#)/TI,AB,CLM
L6 69948 S (395 OR 371 OR 364)/CLAS
L7 8 S L5 AND L6
L8 1 S 4314332/PN
=> d 12 1 cit,ab

1. ~~5,420,992~~ May 30, 1995, Backward-compatible computer architecture with extended word size and address space; **Earl A. Killian**, et al., 395/375; 364/240.3, 258.1, 259.5, DIG.1, DIG.2; 395/500, 800 [IMAGE AVAILABLE]

US PAT NO: 5,420,992 [IMAGE AVAILABLE]

L2: 1 of 3

ABSTRACT:

A technique for extending the data word size and the virtual address space of a pre-existing architecture so that hardware for the extended architecture also supports the pre-existing architecture. Extension of the data word size from m bits to N bits entails widening the machine registers and data paths from m bits to N bits and sign-extending entities of m or fewer bits to N bits when they are loaded into registers. Some of the m-bit instructions, when operating on N-bit sign-extended versions of m-bit entities, produce an N-bit result that may not correspond to the correct m-bit result, sign-extended to N bits. For these instructions compatibility requires that the instructions be further defined to guarantee a sign-extended result. This means that separate N-bit instructions corresponding to these m-bit instructions are needed. The support for up to an N-bit virtual address space is provided in part by widening the virtual address data paths. The extended architecture supports the m-bit architecture's addressing with minimal additional hardware. This is made possible by storing m-bit addresses as N-bit entities in sign-extended form and requiring that the results of address computations on these entities be in sign-extended form.
=> d 13 7 cit,ab

7. 4,679,140, Jul. 7, 1987, Data processor with control of the significant bit lengths of general purpose registers; **Shizuo Gotou**, et al., 395/775; 364/DIG.1 [IMAGE AVAILABLE]

US PAT NO: 4,679,140 [IMAGE AVAILABLE]

L3: 7 of 7

ABSTRACT:

A mode register stores a mode bit for each of the general registers, an access circuit accesses the general registers and the mode register so that a general register designated by an instruction and a corresponding mode bit are read out together. A data use circuit or a data supply circuit connected to the general registers includes a circuit portion which effectively changes the significant bit length of the data read out of the designated general register or of the data to be written into the designated general register.
=> d cit,ab

1. **4,314,332**, Feb. 2, 1982, Memory control system; Yukio Shiraogawa, et al., 395/425; 364/238.4, 240, 240.5, 240.7, 242.3, 242.31, 242.5, 254.9, 259, 259.5, 262.81, 264, 264.6, DIG.1 [IMAGE AVAILABLE]

US PAT NO: **4,314,332** [IMAGE AVAILABLE]

L8: 1 of 1

ABSTRACT:

Disclosed is a memory control system for a data processing system in which the length of an access unit to a memory can be different from the lengths of information words which can be processed and which can include data, addresses, and instructions and operands processed in an arithmetic control apparatus, and combinations thereof. The disclosed memory control system provides an address boundary for effecting a read/write operation with respect to the memory of information words having a half-word length and a full-word length. The half-word length information words can correspond to $2n$ times a minimum word length, n being a positive integer, and the access unit length can be equal to the minimum unit word length. In a disclosed embodiment, the minimum unit word length and the access unit length can be an 8 bit byte. Thus, a half-word length can be 16 bits and a full-word length can be 32 bits.

3. 4,825,355, Apr. 25, 1989, Instruction format for program control type data processing systems; Keiichi Kurakazu, et al., 395/375; 364/232.8, 239, 239.4, 244, 244.3, 244.6, 245, 245.1, 247, 247.6, 262.4, 262.7, 262.8, 262.81, DIG.1 [IMAGE AVAILABLE]

US PAT NO: 4,825,355 [IMAGE AVAILABLE]

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ABSTRACT:

An instruction having two operands includes a field specifying the bit length of a source operand and a field specifying the bit length of data to be operated upon by the execution unit. Based on size information stored in these fields, the operand bit length is modified, which avoids need for modification of the bit length of an operand by use of a macro instruction at the time of execution of an operation based on the two operands. Consequently, the program execution speed can be improved.

1. 5,237,701, Aug. 17, 1993, Data unpacker using a pack ratio control signal for unpacked parallel fixed m-**bit** **width** into parallel **variable** n-**bit** **width** word; Keith J. Bertrand, **395/800**; 341/60, 67, 87; **364/260.4**, **260.7**, **926.1**, **926.3**, **933**, **933.3**, **934.2**, **937.1**, **937.2**, **937.4**, **939.5**, **947**, **947.1**, **947.2**, **947.6**, **948.34**, **950.3**, **951**, **951.1**, **951.5**, **DIG.1**, **DIG.2** [IMAGE AVAILABLE]

US PAT NO: 5,237,701 [IMAGE AVAILABLE]

L7: 1 of 8

ABSTRACT:

The data unpacker receives packed parallel input data words having a fixed width of m bits, and it outputs parallel data words having a **variable** **width** of n **bits**. An input register stores the received words and applies them to a bit shifter. The bit shifter shifts the received data by a number of bit positions indicated by a shift control signal, and the shifted data is output therefrom as a parallel output word having n valid bits. The number n for each output word is received by the unpacker as a binary number. When n **gtoreq** m, a most significant (MSB) bit portion of that number is applied as first MSB control signal. The least significant bit (LSB) portion of n is applied to an adder which adds subsequently received LSB portions to provide a running sum. When the running sum is equal to or greater than m, the adder provides a second MSB control signal, corresponding to the most significant bit of the running sum. The least significant bit portion of the running sum is applied to the bit shifter as the shift control signal. A logic circuit receives the first and second control MSB control signal and it provides in response to either of these signals a READY FOR DATA control signal indicating that the input register is ready to receive the next input word, and a DATA VALID OUT control signal indicating that the bit shifter is ready to output the parallel output word.

2. 4,663,729, May 5, 1987, Display architecture having variable data width; Richard E. Matick, et al., **395/165**; 345/200; **364/926.9**, **926.92**, **935.45**, **935.47**, **964.9**, **DIG.2** [IMAGE AVAILABLE]

US PAT NO: 4,663,729 [IMAGE AVAILABLE]

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ABSTRACT:

A display architecture is disclosed which supports a variable, selectable number of **bits** per chip and a **variable**, selectable segment **width**. The architecture comprises a plurality of dynamic memory chips and a function generator. Each of the memory chips includes at least two data islands wherein each data island has its own data in/out line, chip select and increment bit supplied by the function generator. The function generator receives a starting address X.sub.o, Y.sub.o, the data path width N.sub.D and an encoded segment width S. A bit incrementer in the function generator generates increment bits A.sub.I based on the externally supplied modulo N.sub.D. The function generator generates the physical word address w.sub.o and physical bit address b.sub.o based on the starting address X.sub.o, Y.sub.o, the data path width N.sub.D and the encoded segment width S. Logic circuitry is provided which is responsive to an overflow bit produced by the bit incrementer to control spill and wrap functions. Spill results from the usual bit address incrementing where the data spills from the highest order chip to the

lowest. Wrap is a special case when spill occurs at the right hand edge of the screen and data wraps around on the same scan line to the left hand edge of the screen.

3. 4,291,381, Sep. 22, 1981, Process for running width adjustment; Helmut Siebeck, **395/145**; 354/8 [IMAGE AVAILABLE]

US PAT NO: 4,291,381 [IMAGE AVAILABLE]

L7: 3 of 8

ABSTRACT:

A process for running width adjustment of adjacently positioned characters reduces the spacing of certain characters to enhance the visual impression of composed text. The process classifies the letter and symbols of the font into a plurality of groups according to their suitability for running width adjustment. The amount of running width adjustment to be provided for each pair of adjacent characters is established in accordance with their grouping. During composing, the running width of each character is determined. The characters are classified into the groups. The amount of adjustment to be provided is ascertained by reference to the group of the first character and the group of the second character of each adjacent pair and applied to the running width of one of the characters to reduce the spacing.

4. 4,128,809, Dec. 5, 1978, Time diversity receiver for processing repeatedly received signal bits in consideration of a maximum-level and/or a favorably received signal bit; Kouzou Kage, 375/347; **371/69.1** [IMAGE AVAILABLE]

US PAT NO: 4,128,809 [IMAGE AVAILABLE]

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ABSTRACT:

Responsive to several signal bits carrying an information piece and received with inevitable fluctuations of the signal bit widths and height, a time diversity receiver reproduces the information piece by mainly taking the widest or highest signal bit into consideration. In order to give significance to the widest or highest signal bit, the signal bit levels are added for each information piece. When high-frequency pulses are used to derive the sum width of the signal bit widths, it is preferred to substitute pulses of a frequency equal to a half or so of the high frequency for the high-frequency pulses representative of the width of the signal bit or bits received with serious fluctuations. Alternatively, the transmitter carries out the reproduction by attaching importance to the signal bit received with smallest fluctuations either solely or together with the preference or weight put on the widest or highest signal bit.

5. 3,781,819, Dec. 25, 1973, SHIFT UNIT FOR VARIABLE DATA WIDTHS; Hellmuth R. Geng, et al., **395/425**; **364/715.08**; **926.1**; **926.5**; **947**; **947.1**; **947.6**; **956.4**; **956.5**; **957**; **957.5**; **958**; **958.3**; **DIG.2** [IMAGE AVAILABLE]

US PAT NO: 3,781,819 [IMAGE AVAILABLE]

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ABSTRACT:

A circuit arrangement is provided for controlling a known logical switching network for shifting data of variable widths, wherein the shift amount by which the data bits applied to the input are to be shifted is switched from the true value to the complement value and vice versa by

means of a control signal influenced by control commands, and wherein the partial results thus produced are logically combined to form a further partial result or the final result.

6. 3,751,650, Aug. 7, 1973, VARIABLE LENGTH ARITHMETIC UNIT; William A. Koehn, **364/716**; 341/84 [IMAGE AVAILABLE]

US PAT NO: 3,751,650 [IMAGE AVAILABLE]

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ABSTRACT:

An arithmetic unit in which a plurality of arithmetic and logic functions are performed using either one or both of two inputs X and Y, each input providing a variable number of bits in parallel. The output may be any one of a number of functions, such as the arithmetic functions of $X + Y$ and $X - Y$, and the logical functions $X \text{ sup. } Y$, $X + Y$, $X \text{ .sym. } Y$, X , and Y , etc. All of the functions are generated by the unit and any of the functions may be selected and operate as a data source. The arithmetic unit can operate either in a straight binary or a binary-coded decimal mode. The number of bits in the output for the arithmetic functions is variable and the carry or borrow is generated for each order and is therefore available from the highest order according to the selected length.

7. 3,739,352, Jun. 12, 1973, VARIABLE WORD WIDTH PROCESSOR CONTROL; Roger E. Packard, **395/425**; **364/238.4**; **240.1**; **243**; **243.3**; **243.7**; **245**; **245.1**; **251**; **251.1**; **251.3**; **252.3**; **252.6**; **254.9**; **255.1**; **255.5**; **258**; **258.1**; **259**; **259.3**; **259.5**; **260**; **260.2**; **261.3**; **261.9**; **262.4**; **262.8**; **DIG.1** [IMAGE AVAILABLE]

US PAT NO: 3,739,352 [IMAGE AVAILABLE]

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ABSTRACT:

There is described a microprogrammed processor associated with a free field memory in which operands of any length in terms of the number of bits can be processed. The free field memory is addressed by an address register that points to the boundary between any two bits stored in the memory as the start of a field and that specifies the number of bits in the field up to the maximum bit capacity of the memory. A control register, referred to as a bias register, determines the number of bits in parallel, up to a maximum number of parallel bits accommodated by one memory cycle, required in the execution of particular microinstructions. Any microoperator string involving the manipulation of operands, such as an arithmetic operation or a data transfer operation, includes a bias operation in which the bias register is set to the lesser of the number of bits specified by the address register and the maximum number of bits transferred in one memory cycle. Once the bias register is set, it is used to control internal operations within the processor and transfers between the processor and memory as though the basic width of the machine had been changed.

8. 3,736,414, May 29, 1973, TRANSVERSAL FILTER EQUALIZER FOR PARTIAL RESPONSE CHANNELS; Gerald K. McAuliffe, **364/724.19**; 327/306, 552; 333/18, 28R, 166; **364/724.16**; **819**; 375/232 [IMAGE AVAILABLE]

US PAT NO: 3,736,414 [IMAGE AVAILABLE]

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ABSTRACT:

The present invention relates to a fast converging transversal filter equalizer for partial response channels including a multi-tap delay line. In the preferred embodiment the equalizer multiplies an error signal and a recreated signal as received by the equalizer. The multiplier outputs in turn feed integrators whose outputs represent correlation functions which control the gain from a series of delay line tap outputs, the summation of the tap outputs comprising the output of the equalizer. In a further embodiment of the invention, the error signal is correlated with the tap outputs themselves and the outputs of the correlators control the tap outputs from the delay line to produce the final output signal in a different configuration.